

## Remarks

The withdrawal of the earlier rejections is noted with appreciation.

The claims now stand rejected as being anticipated by or unpatentable over a newly cited Texas Instruments, Inc. publication (herein "TI") that purportedly has a publication date in 1998. Reconsideration and withdrawal of the rejections are respectfully requested for at least the following reasons. As noted below, TI has little, if any, relevance to the claimed subject matter.

TI discloses a UART having an optional serial-bypass mode. This differs from the auxiliary parallel data channel recited in claim 1 in a number of ways.

Firstly, TI discloses a device in which control of host-subsystem communications requires an additional register that is not part of the UART standard. This additional register is the Subsystem Control Register (see page 11). This non-standard register is required to activate the serial-bypass mode (see last paragraph in section headed "Subsystem Control Register" on page 11). Thus, TI does not disclose a register set that is "configurable to control host-subsystem communications according to a UART standard", as recited in feature (a) of claim 1.

Secondly, in TI the serial-bypass mode (as its name suggests) simply bypasses the serial communications link when increased data throughput is required. At times when the serial-bypass mode is enabled, the serial communication channel is disabled and cannot be used. This is because both channels rely on the same internal FIFO buffers, e.g., see under the heading "subsystem serial-bypass mode on page 12. Accordingly, TI also does not teach an interface device having "an auxiliary parallel data communication to the subsystem operable in conjunction with the serial data communication channel", as recited in claim 1. In TI the parallel channel can only be used as an alternative to the serial channel. TI does not allow both the serial and parallel channels to be used simultaneously.

Thirdly, according to claim 1, the parallel interface of the present invention operates under control of the register set (see last line of claim 1). In TI, the serial-bypass mode does not operate under control of the register set. To the contrary, the serial-bypass mode operates by giving the subsystem direct parallel access to the internal UART read and transmit FIFOs (see under the heading "subsystem serial-bypass mode on page 12). That is to say the serial-bypass mode bypasses the registers and does not operate under control of them.

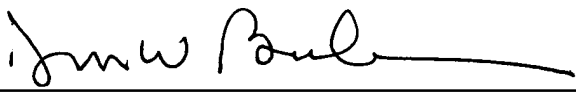
All of the above differences enable interface devices according to the claimed invention to be fully backward compatible with legacy architecture and software code, whereas the interface device of TI is not. The interface device of TI requires specially written software drivers to be implemented. Furthermore, there is nothing in TI which hints or suggests at modifying the disclosed device to include the above-mentioned features which are missing from TI in order to provide a backward compatible device.

Similar comments apply to independent method claim 17. The remaining claims, which recite further features of the present invention, are patentable for at least the same reasons discussed above in respect of independent claim 1.

In view of the foregoing, request is made for timely issuance of a notice of allowance.

Respectfully submitted,

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